

## IN THE CLAIMS

1. (Withdrawn) A charge coupled device comprising:  
a first clocked gate for forming a clocked barrier region, and coupled to a first clocking signal, wherein the clocked barrier region does not store charge; and  
a second clocked gate adjacent to the first clocked gate and coupled to a second clocking signal, the second clocked gate forms a clocked well region, wherein the first clocking signal has a different potential level than the second clocking signal, and the first clocking signal is clocked in phase with the second clocking signal.
2. (Withdrawn) The device of claim 1 wherein the first clocking signal has a lower potential level than the second clocking signal.
3. (Withdrawn) The device of claim 1 further comprising a virtual gate adjacent to second clocked gate.
4. (Withdrawn) The device of claim 1 wherein the virtual gate comprises a virtual barrier and a virtual well.
5. (Withdrawn) The device of claim 1 wherein the second clocked gate overlaps the first clocked gate.
6. (Withdrawn) The device of claim 5 further comprising an insulator layer between the first clocked gate and the second clocked gate.

7. (Withdrawn) The device of claim 1 wherein the device is a frame transfer device.

8. (Withdrawn) The device of claim 1 wherein the device is a full frame device.

9. (Withdrawn) The device of claim 1 further comprising an antiblooming drain.

10. (Withdrawn) The device of claim 9 further comprising an antiblooming barrier adjacent the antiblooming drain.

11. (Currently amended) A charge coupled device comprising:

a first clocked gate coupled to a first clocking signal;

a field plate adjacent to and surrounding the first clocked gate, and coupled to a DC bias source; and

a second clocked gate adjacent to and surrounded by the field plate and coupled to a second clocking signal, the field plate separates the first clocked gate from the second clocked gate, and the first clocking signal is clocked out of phase with the second clocking signal.

12. (Original) The device of claim 11 wherein the first clocked gate comprises a clocked barrier and a clocked well.

13. (Original) The device of claim 12 wherein the second clocked gate comprises a clocked barrier and a clocked well.

14. (Original) The device of claim 11 wherein the device is a frame transfer device.

15. (Original) The device of claim 11 wherein the device is a full frame device.

16. (Original) The device of claim 11 further comprising an antiblooming drain.

17. (Original) The device of claim 11 wherein the device is a charge multiplying device.

18. (Withdrawn) A virtual phase frame interline transfer charge coupled device comprising:

a first clocked gate for forming a clocked barrier region, and coupled to a first clocking signal, wherein the clocked barrier region does not store charge; and

a second clocked gate adjacent to the first clocked gate and coupled to a second clocking signal, the second clocked gate forms a clocked well region, wherein the first clocking signal has a different potential level than the second clocking signal, and the first clocking signal is clocked in phase with the second clocking signal.

19. (Withdrawn) The device of claim 18 further comprising a photo-site region adjacent to the clocked well region.

20. (Withdrawn) The device of claim 19 further comprising a lateral antiblooming drain region adjacent to the photo-site region.